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888 888 888 888	000 000 000 000	000 000 000 000	111 111 111	\$\$\$ \$\$\$ \$\$\$ \$\$\$
888 888 888 888	000 000	000 000	iii	\$\$\$ \$\$\$
888 888888888888	000 000	000 000	iii	\$\$\$ \$\$\$ \$
888888888888 88888888888	000 000	000 000	†††	\$\$\$\$\$\$\$\$\$ \$\$\$\$\$\$\$\$\$
888 888 888	000 000	000 000	111	SSS
888 888 888 888	000 000	000 000	111	\$\$\$ \$\$\$ \$\$\$
888 BBB BBB	000 000	000 000	III	\$\$\$ \$\$\$
888888888888 888888888888 88888888888	00000000 00000000 00000000	00000000 00000000 00000000	111 111 111	\$

KK KK KK

KK

KK KK

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B88BBBBB BBBBBBBB BB BB BB BB BB BB BBBBBBB	000000 00 00 00 00	000000 00 00 00 00
		\$

BOOTBLOCK Table of contents

(2) 50 Declarations BOOSBLOCK - reads in and starts boot code

B

Page

(1)

.TITLE BOOTBLOCK

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FACILITY:

Device-independent boot block for VAX

ABSTRACT:

Reads a file (usually VMB.EXE) off the booting medium into memory and transfers control to the VMB code.

AUTHOR:

23 August 1979 Carol Peters

REVISION HISTORY:

13 Sept 1979 Robert Rappaport Simplified references to local data items.

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E 3 B00\$BLOCK - reads in and starts boot cod 4-SEP-1984 23:40:18 VAX/VMS Macro V04-00 [BOOTS.SRC]BOOTBLOCK.MAR: 1

.SBTTL BOOSBLOCK - reads in and starts boot code

Functional description:

The boot block code reads the primary bootstrap file into physical memory a block at a time. The code calls the device-dependent ROM subroutine once for each block in the bootstrap file. Then the routine jumps to byte 0 of the loaded code.

Inputs:

101

104

106 107

108

109

- type of boot device (UNIBUS) address of the I/O page for the boot device's UNIBUS
- (MASSBUS) address of the device's MASSBUS adapter
 (UNIBUS) 32-bit physical address of the boot device's

 (SR (bits <31:24> must be zero)

 (MASSBUS) adapter's controller/formatter number
 unit number of the boot device R2
- software boot control flags
- physical address of the device-dependent ROM routine that reads an arbitrary LBN into memory R6
- SP - <base_address + ^x200> of 64kb of good memory

Implicit inputs:

UNIBUS adapter map registers 0-127 are mapped to the 64kb of good memory. MR O maps to first page of memory, etc.

The boot block is loaded into the 1st page of the 64KB of memory, i.e. the page which corresponds to MR O.

The first longword (bytes 0-3) of the boot block contains the size of the primary bootstrap.

The second longword (bytes 4-7) contains the starting LBN of the bootstrap file, expressed as swapped words.

The third longword (bytes 8-11) contains the relative offset from the base of the 64KB of memory into which we should load the primary bootstrap program. This must be a positive number less than or equal to 64KB-(size*512) where size is the size of the primary bootstrap.

The starting LBN format is defined by DSC and cannot be changed. The load address is defined by WRITEBOOT and cannot be changed.

Outputs:

- type of boot device (UNIBUS) address of the I/O page for the boot device's UNIBUS
- (MASSBUS) address of the device's MASSBUS adapter R2 - (UNIBUS) 18-bit UNIBUS address of the boot device's

Implicit outputs:

INCL

MOVL

SOBGTR

SP

The routine preserves RO-R1, R3, R4, R5-R6, R8, R10-R11, AP, and SP.

Transfers control to the 0th byte of the primary bootstrap program.

that reads an arbitrary LBN into memory

- <base_address + *X200> of 64kb of good memory

14467890123456789012345667890 1146789012345678901234567890 BOOSBLOCK_CODE: POSHAB FILE_STATS F1 AF F6 AF CO ADDL LOAD_ADDR, (SP) #^M<RO,R4,R5,R8> FILE_SIZE,R4 START_LBN,R8 0131 8F BB D0 B0 B0 PUSHR 54 58 E0 AF E6 AF E6 AF E4 AF MOVL MOVW START_LBN+2, START_LBN MOVW DE AF 58 BO MOVW R8,START_LBN+2 D9 AF D9 AF 10 AE D0 D0 MOVL START_LBN, R8 LOAD_ADDR,R5 MOVL 16(SP) PUSHL 174 175 176 177 READ_BLOCK: 16 E8 00 JSB 01 50 BLBS RO, NEXT_BLOCK HALT NEXT_BLOCK: 00000200 #*X200,R5 #*X200,(SP) ADDL CO 06055 ADDL

AF AF 54 8E

BA B7 E2

Start of device independent code. Move physical address of base of 64KB of memory. Add in relative load address. Result is physical address of load point. Leave on stack for final JMP inst.

8

Save 4 registers for temps. Get # of blocks in VMB. Get upper word value of LBN. Move lower word value of LBN into lower word position. Move upper word value to upper word position. Pickup the swapped LBN.
Get primary boot relative load addr.
Copy physical transfer address to
top of stack for those devices such
as the TUS8 which need physical rather than UNIBUS virtual addresses.

VMB read loop. Call ROM read LBN routine. Branch on successful read. Halt on failure to read.

Read next block. Increment relative address 512 bytes. Increment physical address one page. Increment LBN number. Next LBN is LBN+1. If more blocks, loop. Pop now useless data from stack.

The primary bootstrap program is now in physical memory starting at the specified load address. Restore the saved registers, convert the CSR address to an 18-bit UNIBUS address, and transfer control to the program.

START_LBN START_LBN,R8 R4,READ_BLOCK (SP)+

BOOTBLOCK VO4-000			B00\$	BLOCK	- reads	in an	d starts	G 3 boot cod	15-SEP-1984 4-SEP-1984	23:40:18	VAX/VMS Macro V04-00 Page [BOOTS.SRC]BOOTBLOCK.MAR;1	(3)
5	2	0131 8F FFFC0000 8F 9E	BA CA 17	0053 0053 0057 005E 005E	193 194 195 196 197 198 199 200		POPR BICL JMP .END	#^M <ro.ra #^XFFFCOO a(SP)+</ro.ra 	4,R5,R8> 000,R2	; Rest ; Redt ; CSR ; Jump	tore registers. uce 32-bit (SR to 18-bit that VMB expects. p to primary bootstrap program.	

15-SEP-1984 23:40:18 VAX/VMS Macro V04-00 Page (5

BOOSBLOCK_CODE 0000000C R 01
FILE_SIZE 00000000 R 01
FILE_STATS 00000000 R 01
LOAD_ADDR 00000008 R 01
NEXT_BLOCK 00000039 R 01
READ_BLOCK 00000033 R 01
START_LBN 00000004 R 01

BOOTBLOCK

Symbol table

Psect synopsis

PSECT name

Allocation PSECT No. Attributes

O0000000 (0.) 00 (0.) NOPIC USR CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE BLANK.

BLANK.

Performance indicators

Phase	Page faults	CPU Time	Elapsed Time
Initialization	141	00:00:00.08	00:00:00.29
Command processing	141	00:00:00.60	00:00:02.09
Pass 1	68	00:00:00.55	00:00:01.56
Symbol table sort	0	00:00:00.00	00:00:00.00
Pass 2	68 0 52	00:00:00.39	00:00:01.01
Symbol table output	2	00:00:00.01	00:00:00.01
Psect synopsis output	ī	00:00:00.02	00:00:00.02
Cross-reference output	Ó	00:00:00.00	00:00:00.00
Assembler run totals	301	00:00:01.65	00:00:04.98

The working set limit was 900 pages.
2158 bytes (5 pages) of virtual memory were used to buffer the intermediate code.
There were 10 pages of symbol table space allocated to hold 7 non-local and 0 local symbols.
200 source lines were read in Pass 1, producing 9 object records in Pass 2.
0 pages of virtual memory were used to define 0 macros.

! Macro library statistics !

Macro Library name Macros defined

_\$255\$DUA28:[B00TS.OBJ]B00TS.MLB;1

_\$255\$DUA28:[SYS.OBJ]LIB.MLB;1

_\$255\$DUA28:[SYSLIB]STARLET.MLB;2

TOTALS (all libraries)

O GETS were required to define O macros.

There were no errors, warnings or information messages.

MACRO/LIS=LIS\$:BOOTBLOCK/OBJ=OBJ\$:BOOTBLOCK MSRC\$:BOOTBLOCK/UPDATE=(ENH\$:BOOTBLOCK)+EXECML\$/LIB+LIB\$:BOOTS.MLB/LIB

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